

OpenCL/HLS/Verilog Convolution Implementation Comparison Study

Implementation	Lines of code	Time to compile for emulation	Time to debug code	Time to Optimize
OpenCL Host: .cpp Kernel: .cl	Host: 131 Kernel: 31	Total Time: 6hours approx. Host: 4hours approx. Kernel: 3hours approx. This time includes the time taken to write and successfully compile the code. Does not include the time to remove logical errors.	Total Time: 15 hours approx. Host: 6hours approx. Kernel: 4hours approx. This time includes the time taken to remove logical errors, to understand how to create .exe and .xclbin file and how to force SW_Emulation on SDx. Also includes the time taken to perform multiple test iterations until the right output was achieved	
Vivado HLS	Host (Written in SDx): 154 Kernel (Written in HLS): 42	Total Time: 2.5hours approx. Kernel: 20 mins. approx. Same as used in OpenCL. Added a few pragmas to change the kernel into an AXI interface Host: 2 hours approx. Wrote the host code using ap_int datatypes but got errors and hence had to use standard C /C++ datatypes to resolve the issue	Time to debug: 2.5hours approx. Kernel: 30 mins. approx. Received a few errors in mismatch between the depth of FIFO and the array size in the kernel. Made changes and ran C/RTL co-simulation until it passed on HLS. Host: 2 hours approx. Spent some time in writing the host code. Very similar to the one used in OpenCL. Got a few errors when used ap_int datatype. Hence reverted back to standard C datatypes. The majority of time spent in debugging was waiting for SDx to build the host and kernel code which took roughly a little more than 2 hours.	
Verilog				