

Evaluation of OpenCL design flow for Altera/Intel FPGAs

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- People
 - PI: Kindratenko
 - Users: kindr, rrthakk2, hequ2
- Dates
 - Start date: 02/2017
 - End date: TBD
- Platform(s)
 - [Ac33](#)
- Description
 - Objective
 - Study OpenCL FPGA design flow. Port sample applications and evaluate design flow maturity and ease of use.
 - Abstract
- Status
 - 03/09/17
 - Work in progress. hequ2 and rrthakk2 are re-working on two different applications to OpenCL.
 - 05/16/17
 - done: <https://github.com/Atrifex/CNN-Acceleration>
- Open issues
 - need license to compile for actual hardware

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Application

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